67,200-1226
2003-0776

PRE-CLEAN CHAMBER WITH WAFER HEATING APPARATUS AND METHOD OF USE

Field of the Invention

0001 The present invention generally relates to pre-clean chambers and methods used to pre-clean a surface prior to physical vapor deposition of a metal layer on the surface. More particularly, the present invention relates to a novel pre-clean chamber having a wafer heating apparatus for heating a wafer to optimum processing temperatures during a reactive plasma pre-cleaning process.

Background of the Invention

0002 In the fabrication of semiconductor integrated circuits, metal conductor lines are used to interconnect the multiple components in device circuits on a semiconductor wafer. A general process used in the deposition of metal conductor line patterns on semiconductor wafers includes deposition of a conducting layer on the silicon wafer substrate; formation of a photoresist or other mask such as titanium oxide or silicon oxide, in the form of the desired metal conductor line pattern, using standard lithographic techniques; subjecting the wafer

substrate to a dry etching process to remove the conducting layer from the areas not covered by the mask, thereby leaving the metal layer in the form of the masked conductor line pattern; and removing the mask layer typically using reactive plasma and chlorine gas, thereby exposing the top surface of the metal conductor lines. Typically, multiple alternating layers of electrically conductive and insulative materials are sequentially deposited on the wafer substrate, and conductive layers at different levels on the wafer may be electrically connected to each other by etching vias, or openings, in the insulative layers and filling the vias using aluminum, tungsten or other metal to establish electrical connection between the conductive layers.

0003 Deposition of conductive layers on the wafer substrate can be carried out using any of a variety of techniques. These include oxidation, LPCVD (low-pressure chemical vapor deposition), APCVD (atmospheric-pressure chemical vapor deposition), and PECVD (plasma-enhanced chemical vapor deposition). In general, chemical vapor deposition involves reacting vapor-phase chemicals that contain the required deposition constituents with each other to form a nonvolatile

film on the wafer substrate. Chemical vapor deposition is the most widely-used method of depositing films on wafer substrates in the fabrication of integrated circuits on the substrates.

0004 Physical vapor deposition (PVD) is another technique used in the deposition of conductive layers, particularly metal layers, on a substrate. The most common forms of PVD are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. Evaporation and e-beam evaporation were used extensively in the manufacture of earlier generations of medium and large scale integrated circuits, but have since been replaced by sputtering, in which semiconductor wafers are produced by the deposition or "sputtering" of a metallic layer on the surface of a silicon wafer.

0005 PVD systems typically include a first air lock loading chamber in which cassettes containing a plurality of wafers to be processed are placed and from which the wafers are transported to a second vacuum chamber (or transportation chamber) using a conveyor. Subsequently, the wafers are placed on a rotating table or stage in the plasma deposition chamber. After the deposition process, the processed wafers are again

transported back through the transportation chamber, to the loading chamber and then back into the cassette for further handling or processing.

0006 A commonly-used technique in semiconductor fabrication which utilizes the PVD layer deposition method is the dual damascene process. In the dual-damascene process flow, a bottom dielectric layer is deposited over a wafer and over a metal interconnect line previously deposited in or on the wafer; an etch stop layer, typically SiN, is deposited on the bottom dielectric layer; and a top dielectric layer is deposited on the etch stop layer. A via opening is etched through the top dielectric layer, the etch stop layer and the bottom dielectric layer, above the metal interconnect line. A trench opening is then etched in the top dielectric layer to the etch stop layer, above the via opening.

0007 Next, a barrier material of Ta or TaN is deposited on the sidewalls and bottoms of the trenches and vias using ionized PVD. A uniform copper seed layer is then deposited on the barrier layer using CVD. After the trenches and vias are filled with copper, the copper overburden extending from the trenches

is removed and the upper surfaces of the metal lines planarized using CMP. In one type of dual damascene process, the vias and the trenches are etched in the same step, and the etch stop layer defines the bottom of the trenches. In other variations, the trenches are patterned and etched after the vias.

0008 Prior to physical vapor deposition of the barrier layer to the sidewalls and bottom of the trench and via, the wafers undergo a pre-clean process in a pre-clean chamber to remove any chemical residue or oxide which may be formed when the wafer is exposed to the atmosphere. Any chemical residue or oxide which remains on the wafer can act as a dielectric shield and impede the PVD film from uniformly adhering to the surface. The pre-clean chamber applies a light, non-selective, non-reactive plasma etch to the wafer to remove chemical residues, such as Cu2O, CuO, Cu(OH)2 , CuCO3 and CuFx remaining on the wafer surface. It also removes a thin layer of oxide formed on the surface of the wafer when the wafer is exposed to the atmosphere, and exposes a fresh metal surface prior to the metallization step.

0009 A typical conventional pre-clean chamber 100 is shown in Figure 1. The pre-clean chamber 100 includes a base 102 and a chamber wall 104 that includes a wafer port (not shown) for transport of a wafer W into the chamber 100. The wafer W is transferred to a wafer lift 106, which includes a wafer pedestal 108, an insulator 110, an insulator base 118, a shaft 120 and a bellows assembly 112. The wafer pedestal 108 is an RF-biased, disk-shaped platform made of aluminum, titanium or other non-reactive metal. The wafer pedestal 108 is supported and insulated by the insulator 110. The insulator 110 is generally a one-piece insulative material such as ceramic or quartz. The insulator 110 insulates the sides and bottom of the wafer pedestal 108 and collimates the RF power to the top surface of the wafer pedestal 108 and, hence, through the wafer W. The insulator 110 is supported by the insulator base 118. The shaft 120 supports the wafer pedestal 108, the insulator 110 and the insulator base 118 and moves the wafer W vertically between a release position, where the wafer W is introduced into and removed from the the transport chamber, and a processing position, where the wafer W is maintained during the etching process. The bellows assembly 112 surrounds the shaft 120 and isolates the shaft 120 when the chamber 100 is under vacuum. A

chamber cover 116 covers and seals the chamber 100 during wafer processing.

0010 During pre-cleaning of the wafer W, argon gas or other gases is/are introduced into the chamber 100. Source RF power is then applied to the chamber 100, causing high voltage and high current to strike an argon plasma in the chamber. When the source RF power is supplied to the chamber 100, the bottom surface of the chamber cover 116 acts as an anode and the wafer pedestal 108 acts as a cathode. Positively-charged argon ions are attracted to the negatively-charged wafer pedestal 108. These ions bombard the wafer W on the wafer pedestal 108 and vertically etch the wafer surface.

0011 During the dual damascene process, the metal interconnect line previously fabricated in or on the wafer is exposed at the bottom of the via opening. Consequently, the high temperatures inherent in the argon plasma pre-clean process frequently result in re-sputtering of metal from the metal interconnect line onto the sidewalls of the via opening. This degrades the electrical performance of devices fabricated on the wafer.

0012 As device features shrink in size with advances in semiconductor fabrication technology, the argon plasma pre-cleaning process is no longer a viable approach to the pre-cleaning of via and trench sidewall and bottom surfaces. Reactive pre-cleaning of these surfaces using hydrogen plasma, however, is a viable pre-cleaning alternative. Optimum efficiency using the hydrogen plasma reactive pre-cleaning process requires heating of the wafer to a relatively high temperature (>200 degrees C) which cannot be attained using the conventional pre-clean chamber design, since the conventional pre-clean chamber does not include a mechanism for directly heating wafers.

0013 In current hydrogen plasma reactive pre-cleaning practice, wafers are initially heated in a degassing chamber, in which adsorbed water vapor, oxygen and other gases are removed from the trench and via surfaces. In the degassing chamber, the wafers are pre-heated to the processing temperature required for the subsequent hydrogen pre-cleaning step. Next, the wafers are removed from the degassing chamber and transferred into the pre-clean chamber. However, this practice is attended by obvious disadvantages, among which are a reduction in wafer throughput

and a compromise in the pre-cleaning efficiency. Furthermore, the wafers tend to cool during transfer from the degassing chamber to the pre-clean chamber. Accordingly, a novel pre-clean chamber is needed to heat a wafer to the processing temperatures required to facilitate optimum pre-cleaning efficiency during hydrogen pre-cleaning of a surface in a dual damascene or other semiconductor fabrication process.

0014 An object of the present invention is to provide a novel pre-clean chamber having a wafer heating apparatus for heating a wafer during a pre-clean process.

0015 Another object of the present invention is to provide a novel pre-clean chamber in which the functions of degassing and pre-cleaning may be combined.

0016 Still another object of the present invention is to provide a novel reactive pre-clean chamber having a wafer heating apparatus for the direct heating of wafers in the chamber.

0017 Yet another object of the present invention is to provide a novel reactive pre-clean chamber having a high-temperature

electrostatic chuck (HTESC) for the heating of wafers in the chamber.

0018 A still further object of the present invention is to provide a novel RPC (reactive pre-clean) method.

0019 Yet another object of the present invention is to provide a novel wafer processing method which includes a degassing process and a reactive pre-cleaning process combined in a single chamber.

Summary of the Invention

0020 In accordance with these and other objects and advantages, the present invention is generally directed to a novel reactive pre-clean chamber that contains a wafer heating apparatus, such as a high-temperature electrostatic chuck (HTESC), for directly heating a wafer supported on the apparatus during a pre-cleaning process. The wafer heating apparatus is capable of heating the wafer to the optimum temperatures required for a plasma reactive pre-clean (RPC) process. Furthermore, degassing and pre-cleaning can be carried out in the same pre-clean chamber.

0021 The present invention is further directed to a method for degassing and pre-cleaning a wafer. The method includes providing a wafer; providing a pre-clean chamber containing a wafer heating apparatus; placing the wafer on the wafer heating apparatus in the pre-clean chamber; heating the wafer to an optimum temperature required for pre-cleaning of the wafer; degassing the wafer and subjecting the wafer to a plasma reactive pre-cleaning process; and removing the wafer from the pre-clean chamber.

0022 The present invention may further include a method for degassing and pre-cleaning trench and via sidewalls etched in dielectric layers provided on a wafer. The method includes providing a wafer having dielectric layers deposited thereon; providing a pre-clean chamber containing a wafer heating apparatus; placing the wafer on the wafer heating apparatus in the pre-clean chamber; heating the wafer to an optimum temperature required for pre-cleaning of the wafer; degassing the wafer and subjecting the wafer to a hydrogen plasma reactive pre-cleaning process; removing the wafer from the pre-clean chamber; depositing a barrier layer on the trench and via sidewalls; depositing a seed layer on the barrier layer; and

filling the trench openings and via openings with a metal such as copper, typically using ECP (electrochemical plating).

Brief Description of the Drawings

0023 The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

0024 Figure 1 is a schematic of a typical conventional pre-clean chamber used to pre-clean semiconductor wafers;

0025 Figure 2 is a schematic of a pre-clean chamber with wafer heating apparatus of the present invention; and

0026 Figure 3 is a flow diagram illustrating a typical flow of sequential process steps in implementation of the method according to the present invention.

Detailed Description of the Invention

0027 The present invention contemplates a novel pre-clean chamber having a wafer heating apparatus which directly applies thermal energy to a wafer supported on the apparatus during a pre-cleaning process. The wafer heating apparatus is

particularly advantageous in heating the wafer to the optimum temperatures required for a typically hydrogen or ammonia reactive plasma pre-clean (RPC) process. In a preferred embodiment, the wafer heating apparatus is a high-temperature electrostatic chuck (HTESC). A dielectric degassing step can be combined with the pre-cleaning step in the pre-clean chamber.

0028 The present invention further contemplates a method for degassing and pre-cleaning a wafer. The method includes providing a semiconductor wafer which may have first and second dielectric layers deposited thereon and trench and via openings etched in the dielectric layers, in a partially-fabricated dual damascene structure on the wafer. The wafer is placed on the wafer heating apparatus in the pre-clean chamber. The wafer is then heated to an optimum temperature required for pre-cleaning of the wafer, and is then subjected to a reactive hydrogen or ammonia plasma pre-cleaning process. Simultaneously, the wafer is subjected to a degassing step in which water vapor, oxygen and other gases are driven from the wafer surface or dielectric layers on the wafer prior to deposition of a barrier layer on the wafer or on the trench and via sidewalls of the dual damascene structure.

0029 In the fabrication of a dual damascene structure, a metal interconnect line is deposited on a wafer substrate beneath each via opening and trench opening. During the reactive pre-cleaning (RPC) process, the wafer is preferably subjected to a process temperature of greater than typically about 350 degrees C. Such a temperature provides the widest possible process window for the RPC process. However, a process temperature of greater than about 350 degrees C has a tendency to result in the formation of a hydride layer on the typically copper surface of the metal interconnect line in the dual damascene structure, resulting in an electrical resistance which is higher than that of pure copper. Accordingly, a process temperature of typically at least about 150 degrees C is sufficient for optimum pre-cleaning of the wafer surface or trench and via sidewalls of the dual damascene structure.

0030 Referring to Figure 2, an illustrative embodiment of the pre-clean chamber with wafer heating apparatus of the present invention is generally indicated by reference numeral 1. The pre-clean chamber 1 typically includes a base 2 and a chamber wall 4 that includes a wafer port (not shown) for transport of a wafer W into the chamber 1. The base 2 is closed by a removable

lid 16 and defines a chamber interior 5. A wafer lift 6 in the chamber interior 5 includes an insulator base 18; an insulator 10 provided on the insulator base 18; and a wafer heating apparatus 8 provided on the insulator 10 for supporting a wafer W (shown in phantom). The insulator 10 may be a one-piece insulative material such as ceramic or quartz which supports and insulates the wafer heating apparatus 8. The insulator 10 also collimates RF power to the top surface of the wafer heating apparatus 8 and, hence, through the wafer W.

0031 The wafer lift 6 typically further includes a shaft 20 which supports the insulator base 18, the insulator 10, and the wafer heating apparatus 8 in the chamber 1. The shaft 20 is operable to move the wafer W vertically between a release position, at which the wafer W is introduced into and removed from a transport chamber (not shown), and a processing position, where the wafer W is maintained during the etching process. A bellows assembly 12 may surround the shaft 20 and isolate the shaft 20 when the chamber 1 is under vacuum. The chamber cover 16 covers and seals the chamber 1 during wafer processing. A source RF power supply 30 is operably connected to the chamber 1 to generate source RF power in the chamber 1.

0032 The wafer heating apparatus 8 is preferably a high-temperature electrostatic chuck (HTESC). A bias RF power supply 26 is connected to the wafer heating apparatus 8 to apply RF bias energy to the wafer W. A temperature controller 22 is operably connected, typically through suitable wiring 24, to the wafer heating apparatus 8 for the purpose of heating and maintaining the wafer heating apparatus 8 at a selected temperature, according to the knowledge of those skilled in the art.

0033 During pre-cleaning of the wafer W, as hereinafter further described, the wafer heating apparatus 8 heats the wafer W to the selected processing temperatures for optimum pre-cleaning of the wafer W. Hydrogen or ammonia gas 28 is introduced into the chamber 1 through the gas inlet 14. Source RF power is applied to the chamber 1 by the source RF power supply 30, causing high voltage and high current to strike a hydrogen or ammonia plasma in the chamber 1. When the source RF power is supplied to the chamber 1, the bottom surface of the chamber lid 16 acts as an anode and the wafer heating apparatus 8 acts as a cathode. Positively-charged ions are attracted to the negatively-charged wafer pedestal 8. These ions bombard the wafer W on the wafer

heating apparatus 8 and vertically etch the wafer surface. Simultaneously, the bias RF power supply 26 may be used to apply an RF bias to the wafer heating apparatus 8, thereby accelerating the collision of ions with the surface of the wafer W and enhancing the pre-cleaning process, as deemed necessary.

0034 Referring next to the flow diagram of Figure 3, wherein a typical flow of process steps according to the method of the present invention is shown. The pre-clean chamber 1 of the present invention is particularly applicable in the pre-cleaning of trench and via sidewalls prior to deposition of a metal barrier layer on the sidewalls, in the fabrication of a dual damascene structure. However, the chamber 1 may also be used to pre-clean surfaces on a wafer in a variety of semiconductor fabrication processes.

0035 In process step 1, trench openings and via openings are etched in dielectric layers previously deposited on a semiconductor wafer. This is carried out by patterning a photoresist layer on each dielectric layer and etching the trenches and vias in the respective layers, as is well-known by those skilled in the art. After the trench and via openings are

etched in the dielectric layers, the photoresist is stripped from the layers.

0036 In process step 2, the wafer W is placed on the wafer heating apparatus 8 in the pre-clean chamber 1, as shown in Figure 2. In process step 3, the wafer W is simultaneously subjected to pre-cleaning and degassing. Accordingly, the temperature controller 22 is used to heat the wafer heating apparatus 8 and wafer W to a target processing temperature which is optimum for pre-cleaning of the trench and via sidewalls etched in the dielectric layers on the wafer W. Preferably, the wafer heating apparatus 8 is used to heat the wafer W to a temperature of at least typically about 150 degrees C. Most preferably, the wafer W is heated to a temperature of at least about 350 degrees C.

0037 After the wafer W is heated to the target processing temperature, hydrogen or ammonia gas 28 is introduced into the chamber 1 through the gas inlet 14. Source RF power of typically about larger than 200 watts is applied to the chamber 1 to ionize the hydrogen or ammonia gas and form a plasma in the chamber 1. A bias RF power of typically about 0-400 watts is

applied to the wafer W by the RF bias 26. Accordingly, positive ions formed in the plasma strike the trench and sidewalls on the negatively-charged wafer W, thereby etching chemical residues and oxides from the sidewalls. Also, gases such as water vapor and oxygen are driven from the trench and via sidewalls as those surfaces are degassed at a temperature of typically about 300 degrees C. The pre-cleaning and de-gassing step 3 is continued for a time period of typically about 30-120 minutes to ensure optimum pre-cleaning and degassing of the trench and via sidewalls prior to subsequent deposit of a metal barrier layer on those surfaces.

0038 In process step 4 of Figure 3, the wafer W is removed from the pre-clean chamber 1. In process step 5, a metal barrier layer is deposited on the trench and via sidewalls and bottoms. This step usually involves deposition of a Ta or TaN layer on the bottom and sidewalls of the trench and vias using an ionize PVD process, according to the knowledge of those skilled in the art.

0039 In process step 6, a metal seed layer, typically copper, is deposited on the metal barrier layer. This step is typically

performed using a conventional CVD process. In process step 7, the trenches and vias are filled with copper, typically using conventional electrochemical deposition (ECD) techniques. Finally, the dual damascene structure is completed by subjecting the copper to CMP (chemical mechanical planarization) to remove copper overburden from the structure.

0040 While the preferred embodiments of the invention have been described above, it will be recognized and understood that various modifications can be made in the invention and the appended claims are intended to cover all such modifications which may fall within the spirit and scope of the invention.